

REMARKS

Claims 1 to 8 are pending. Claims 1 to 8 have been rejected. Claims 1, 2, 4, 6, and 8 are amended. The amendments to claims 1 and 4 were made to clarify the claims. The amendments do not narrow the scope of the claims.

Objection to Specification

The Office Action essentially states:

The disclosure is objected to because of the following informalities:

(a) On page 13, lines 4, a high strain region "1210" should be --1210a -1210c -- and the die corner "1200" should be --1200a -1200c--.

(b) "soldermask" should be --solder mask--.
Appropriate correction is required.

Applicants have amended the specification and Abstract to overcome these objections.

Objection to Drawings

The Office Action essentially states:

Figures 1, 2a, 2b, 5a and 5b should be designated by a legend such as -- Prior Art -- because only that which is old is illustrated. See MPEP § 608.02(g).

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "355" in Fig. 3 and "455" in Fig. 4 have been used to designate both solder ball and chip (see page 8, line 7 and page 10, line 1).

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because:

a) they do not include the following reference sign(s) mentioned in the description:

- i) In Fig. 5a, reference numeral "530a, 510a, 560a and 520a" are not disclosed in the specification.
- ii) In Fig. 11a, reference numeral "1210a and 1200a" are not disclosed in the specification.
- iii) In Fig. 11b, reference numeral "1210b and 1200b" are not disclosed in the specification.
- iv) In Fig. 11c, reference numeral "1210c and 1200c" are not disclosed in the specification.

b) they do not include the following reference sign(s) mentioned in the description:

- i) On page 10, line 24, the stiffener ring "530" is not referenced in the figures.
- ii) On page 11, line 2, the gap "560", the die "510" and the stiffener ring "530" are not referenced in the figures.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitation "the substrate board attach surface comprises at least one solid plane covering the chip attach surface region near at least one chip corner" in claims 1 and 4 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121 (d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Applicants have designated Figs. 1, 2a, 2b, 5a, and 5b as Prior Art to overcome the objection. Applicants have amended the Specification to overcome the remaining objections.

Claim Objections

Claims 2, 6 and 8 objected to because of the following informalities: "soldermask" should be --solder mask--. Appropriate correction is required.

Applicants have amended claims 2, 6, and 8.

§ 102 Rejections

Applicants respectfully submit that according to MPEP 2131 "[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." (citing *Verdegall Bros. V. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)).

Claim 1 stands rejected under 35 USC § 102(b) as being anticipated by Davies et al. (U.S. Pat. No. 5,901,041).

The Office Action essentially states:

Regarding claim 1, Davies et al. discloses in e.g., Fig. 2 and Fig. 3 a laminated flip-chip interconnect package (a package 10 in Fig. 1, Fig. 4 and column 3, lines 15 -46) comprising

- a substrate (14; column 3, lines 16 -19) having a chip (12; column 3, lines 34 -35) attach surface (32) and a board (PCB 40; column 4, lines 30 -31) attach surface (34) that define contact pads (pads under the flip-chip solder balls 80 in Fig. 4 and pads on the solder balls 16) for attachment to corresponding pads on the chip and board (see Fig. 3 and Fig. 4),
- wherein the substrate board attach surface (34) comprises at least one solid plane (24) covering the chip attach surface region near at least one chip corner,
- said solid plane comprising a dielectric material (epoxy 24; column 3, lines 60 -61).

Applicants submit that the solid plane referred to in the office action is a lower molded body (24) that is sealed to the surface (34) of tape (14). See Davies, col. 3, lines 46-61. The

office action identifies surface (34) as the board attach surface. Lower molded body (24) is not an area of the board attach surface and, therefore, cannot be a solid plane area of the board attach surface.

Furthermore, Applicants have amended claim 1 to state that the board attach surface includes contact pads opposite a chip attach location and adjacent regions on the chip attach surface except for at least one solid plane area of the board attach surface, the area being opposite a chip attach surface region adjacent a corner of a chip attach location. Davies does not disclose this feature. Accordingly, the reference does not describe every element of the claimed invention.

For these reasons, Applicant(s) submit that the cited reference will not support a 102(b) rejection of the claims invention and request that the rejection be withdrawn.

Claims 1-3 stand rejected under 35 USC § 102(e) as being anticipated by Farquhar et al. (U.S. Pat. No. 6,600,244):

The Office Action essentially states:

Regarding claim 1, Farquhar et al. discloses in e.g., Figs. 1a -1c and column 4, lines 1-30 a laminated flip-chip interconnect package (16) comprising

- a substrate (16) having a chip (10 in Fig. 1c; column 5, lines 24 -25) attach surface and a board (26; column 5, lines 39 -40) attach surface that define contact pads (22 and the pads the top surface of the element 16 for the chip 10 in Fig. 1c) for attachment to corresponding pads on the chip and board (see Fig. 1c),
- wherein the substrate board attach surface (the surface that has the element 22) comprises at least one solid plane (18) covering the chip attach surface region near at least one chip corner (see Fig. 1c),
- said solid plane comprising a dielectric material (the top dielectric adhesive layer in the adhesive coated polyimide spacer 18; column 3, lines 30 -34).

Regarding claim 2, Farquhar et al. discloses in e.g., Figs. 1a -1c and column 4, lines 1-30 said dielectric material (the top dielectric adhesive layer in the adhesive coated polyimide spacer 18) being covered with a layer of a coverlay material (the polyimide layer; column 4, lines 14 -15).

Regarding claim 3, Farquhar et al. discloses in e.g., Figs. 1a -1c and column 4, lines 14-15 said layer of material being polyimide.

Applicants submit that the solid plane referred to in the office action is a spacer and adhesive (18) that is attached to the surface of thin film (16). See Farquhar at col. 5, lines 33-43. The office action identifies a surface of thin film (16) as the board attaché surface. Spacer and

adhesive (18) is not an area of the board attach surface and, therefore, cannot be a solid plane area of the board attach surface.

Furthermore, Applicants have amended claim 1 to state that the board attach surface includes contact pads opposite a chip attach location and adjacent regions on the chip attach surface except for at least one solid plane area of the board attach surface, the area being opposite a chip attach surface region adjacent a corner of a chip attach location. Farquhar does not disclose this feature. Accordingly, the reference does not describe every element of the claimed invention.

For these reasons, Applicant(s) submit that the cited reference will not support a 102(e) rejection of the claims invention and request that the rejection be withdrawn.

Claims 4-6 stand rejected under 35 USC § 102(b) as being anticipated by Lau (U.S. Pat. No. 6,075,710).

The Office Action essentially states:

Regarding claim 4, Lau discloses in e.g., Fig. 3, Fig. 4A and column 4, line 58 –column 5, line 15 a laminated flip-chip interconnect package (100; column 1, line 67 -column 2, line 2) comprising

- a substrate (110) having a chip attach surface (the surface that is connected a chip 105) and a board attach surface (the surface that is connected to the PCB 150) that define contact pads (the pads on the both surfaces) for attachment to corresponding pads on the chip and board,
- wherein the substrate board surface comprises at least one solid plane (130 at the left corner in Fig. 3) covering the chip attach surface region near the chip corners (see Fig. 3),
- said solid plane comprising a metal (copper 130; column 5, lines 38 -40).

Regarding claim 5, Lau discloses in e.g., Fig. 3 and Fig. 4A said metal being copper (copper 130; column 5, lines 38 -40).

Regarding claim 6, Lau discloses in e.g., Fig. 3 and Fig. 4A said metal (130 at the left corner in Fig. 3) being covered with a layer of a soldermask (155; column 5, lines 65 -66).

Regarding claim 8, Lau discloses in e.g., Fig. 3 and Fig. 4A said soldermask (155) having a plurality of openings defining ball grid array pads (130 except the 130 at the left corner in Fig. 3).

Applicants submit that the solid plane referred to in the office action is a land grid array (130) disposed on the bottom surface of substrate (110). *See* Lau at col. 5, lines 19-23. The office action identifies a surface of substrate 110 as the board attach surface. Land grid array 130 is not an area of the board attach surface and, therefore, cannot be a solid plane area of the board attach surface.

Furthermore, Applicants have amended claim 1 to state that the board attach surface includes contact pads opposite a chip attach location and adjacent regions on the chip attach surface except for at least one solid plane area of the board attach surface, the area being opposite a chip attach surface region adjacent a corner of a chip attach location. Lau does not disclose this feature. Accordingly, the reference does not describe every element of the claimed invention.

For these reasons, Applicant(s) submit that the cited reference will not support a 102(b) rejection of the claims invention and request that the rejection be withdrawn.

§ 103 Rejections

Claim 7 stands rejected under 35 USC § 103(a) as being unpatentable over Lau in view of Knapp et al. (U.S. Pat. No. 5,973,337).

The Office Action essentially states:

While Lau teaches the use of the soldermask material, Lau does not appear to provide any example of the soldermask's specific composition. Knapp et al. teaches in e.g., Fig. 1 and column 2, lines 50 -51 the soldermask material (23) may be composed of a polyimide. It would have been obvious to one of ordinary skill in the art at the time when the invention was made to apply the polyimide as the specific material to form the soldermask material at the bottom surface of the interposer of Lau as taught by Knapp et al. (1) to reduce cost of manufacture by using a low cost polymer material (i.e., polyimide), (2) to provide an excellent heat resistance and radiation resistance polymer at cryogenic temperatures and (3) to provide a liquid soldermask material (column 2, lines 50 -51).

Applicants respectfully submit that according to MPEP 2142, to establish a case of *prima facie* obviousness, three basic criteria must be met: 1) there must be some suggestion or motivation, either in the references or generally known to one skilled in the art, to modify or combine reference teachings, 2) there must be reasonable expectation of success, and 3) prior art references must teach or suggest all the claim limitations. The ability to modify the method of the references is not sufficient. The reference(s) must provide a motivation or reason for making the changes. *Ex parte Chicago Rawhide Manufacturing Co.*, 226 USPQ 438 (PTO Bd. App. 1984).

Applicants respectfully submit that the references cannot support a case of *prima facie* obviousness as to the amended claims because, among other possible reasons, the cited references do not provide a motivation or suggest for at least one area of a board attach surface having contact pads opposite a chip attach location and adjacent regions on the chip attach

surface except for at least one solid plane area of the board attach surface, the area being opposite a chip attach surface region adjacent a corner of a chip attach location. In addition, these references do not disclose all the elements of the present invention because they do not disclose contact pads opposite a chip attach location and adjacent regions on the chip attach surface except for at least one solid plane area of the board attach surface, the area being opposite a chip attach surface region adjacent a corner of a chip attach location.

For these reasons, Applicant(s) submit that the cited references will not support a 103(a) rejection of the claims invention and request that the rejection be withdrawn.

In addition to the foregoing arguments, Applicant(s) submit that a dependent claim should be considered allowable when its parent claim is allowed. *In re McCairn*, 1012 USPQ 411 (CCPA 1954). Accordingly, provided the independent claims are allowed, all claims depending therefrom should also be allowed.

Based on the foregoing, it is submitted that the application is in condition for allowance. Withdrawal of the rejections under 35 U.S.C. 102 and 103 is requested. Examination and reconsideration of the claims are requested. Allowance of the claims at an early date is solicited.

Respectfully submitted,

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Date

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Amendments to the Drawings:

The attached sheet of drawings includes changes to Figs. 1, 2a, 2b, 5a, and 5b.